LM002
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Medtronic

INVENTION DISCLOSURE FORM

WARNING: Due to the confidential nature of this document, save it as a password protected document. Do not send this document through GroupWise.

This is a WORD Template form. Press enter or tab to move to each field. Please fill out this form as completely as possible. If the allotted space is not sufficient, use a separate sheet. Have your manager sign the form and forward it to the Patent Section of the Law Department, MS301. Please attach any drawings and technical descriptions that are available and assemble copies of the background articles, books, advertisements, etc. for use by your patent attorney.

1.

Inventor(s) Full Name(s)	Employee Number	Mail Stop	Home Address (Include Zip Code)
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2. Title of Invention: Bumpable 1KV DMOS Device.

3. Summary of the Invention: 1000V vertical mosfet, which is bumped, having a drain contact on the front surface of the die. Drain contact is made via a trench through the epi region down into the substrate. The mosfet obtains a low Rdson by having a high cell packing density, thus creating a multitude of current paths in parallel.

4. How have others addressed this problem (List and attach any patents, books, articles, devices, Medtronic or competitor's products, or other background materials you used or which may be prior art)? wire bond or other chip carriers

5. The invention is described on pages _____ of Lab Notebook No. _____ (Please attach copy).

   See Medtronic Microelectronics Center Specification 3212963.

6. When was a device built which included the invention? Development is underway.

   Who built it? Medtronic Microelectronics Center Where is it? 2343 W. 10th Place, Tempe, AZ 85281

   Who has supporting documents? SST Organization has design rule flow and Wafer Fab has a Promis Process Flow

   Who witnessed tests? _____ When and where? _____

7. Discuss the problems which the invention is designed to solve, referring to any prior devices of a similar nature with which you may be familiar. The invention provides a 1KV DMOS device which can be solder reflow attached to a circuit board. This invention eliminates the need for wirebondable devices.

8. State the advantages of the invention over presently known devices, systems or processes. The invention provides a bumped, surface mountable 1KV DMOS device.

9. List all known and other possible uses for the invention. Other applicable high voltage device technologies

10. Specifically describe the invention and its operation. You may use and attach copies of sketches, prints, photographs and illustrations which should be signed, witnessed and dated. Use numbers and descriptive names in descriptions and drawings. See attached description and drawings

11. List all features of the invention that are believed to be novel. Etches in the <100> surface orientation to create a "trench" in the epitaxial silicon, allowing contact to the substrate-drain of the device (see Figure 1). A bumped 1KV DMOS vertical mosfet.

12. Sale or Publication (Needed to establish the date of any printed publication, public use or sale, since no U. S. patent application may be filed after one year from such date.)

Bumpable 1KV DMOS Device

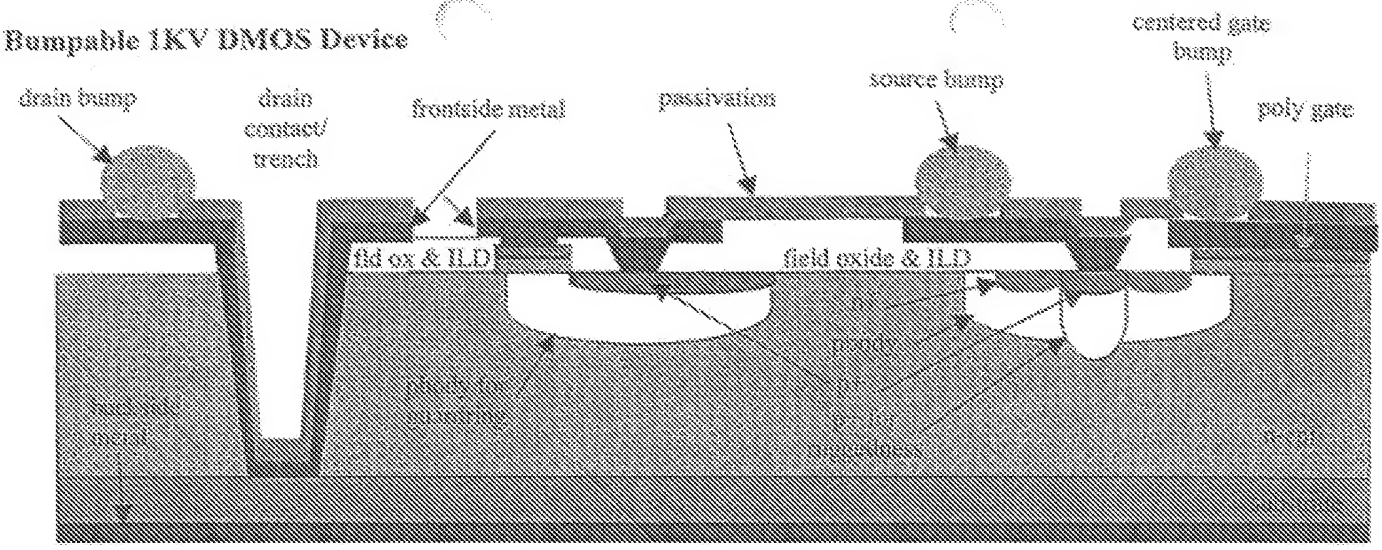

Figure 1 – Bumpable 1KV DMOS Device Simplified Cross Section

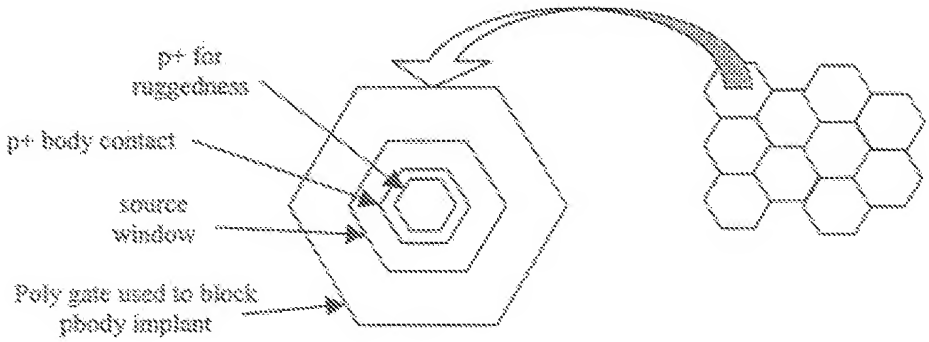

Figure 2 – Packing Density of the Hexagonal MOSFET Cell Contruction with Expanded View of Layout Cell

DEVICE CLAIMS (General)

1. Trench etched in the <100> crystal orientation; Allows drain-substrate contact.
2. Centered Gate Bump allows a more consistent gate voltage across the die.
3. Metal on backside of wafer reduces Rdson of DMOS device.
4. Plurality of cells to maximize packing density of DMOS cells by using hexagonal cell construction.
5. Allows for smaller hybrid packaging area by eliminating the need for wire bonds and the space surrounding the die.
6. Field plates in the guardrings contact both metal and poly to alter the surface field potential.
7. Uses the patterned polysilicon as a blocking mask for the pbody implant.
8. For use in implantable medical devices.

Taken together we believe that the above claims, or subset, may be patentable.

DEVICE CLAIMS (Specific)

1. Device having a pbody diffusion junction depth between 6-9um.
2. Device having a p+ junction extending slightly farther than the pbody diffusion for improved avalanche/ruggedness.
3. Device having a p+ source/drain implant overlapping the n+ source region for use as a body contact.
4. Device having a poly gate width between 19-22um.
5. Device having a mosfet cell pitch between 30-40um.
6. Device having a threshold voltage between 2 and 4 volts.
7. Device having an on state resistance (Rdson) of less than approximately 0.8 micro-ohms/micron^2.
8. Device having the ability to hold off a minimum of 1000 volts drain to source.

a. If a device has been offered, or will be offered for sale, or used for profit or otherwise publicly disclosed, state when and to whom delivered and how used? n/a

b. Has a printed description of this invention been made available to persons outside the company? How and when and was use restricted (e.g. licensing agreement, non-disclosure agreement, proprietary legends, etc.)?

Non-Disclosure Agreement

- Provided METAL and PAD data to facilitate manufacture of the bump stencil.
- Test wafer(s) were sent to facilitate verification of the bump stencil.
- Discussed bumping near the drain contact/trench.

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13. Inventor(s) Signature(s) (REQUIRED):

Signature	Date
	[redacted]

Manager's Comments

14. How is this invention important to your products, plans or goals?

FLIP CHIP HIGH POWER COMPONENTS ARE AN IMPORTANT FEATURE FOR SIMPLIFYING THE HYBRID ASSEMBLY PROCESS. HAVING ALL DIE BE SURFACE MOUNT FOR BOTH LOW VOLTAGE AND HIGH VOLTAGE ON ONE HYBRID IS DESIRABLE.

15. Manager's Signature (REQUIRED)

Signature

Date [redacted]

Manager's Printed Name PAUL F. GERRISH

Mail Stop 20-6

Business Unit CRM / MMC

Manager: Please forward to Patent Section of Law Department, MS 301, upon completion of your review.

```
$GDPDC          DCOP    Z003G.04
                Entry constraint: DONTCARE/DONTCARE/DONTCARE/DONTCARE
                Exit constraint:  NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
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$PADE           STRING  PAD
$PAVIMP         STRING  WZ250-B11_2E15@35KEV
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$R5             STRING  WTCBS-R5A
$R6             STRING  WTCBS-R6A
$R61            STRING  WTCBS-R61A
$R75            STRING  WTCBS-R75A
$R8             STRING  WTCBS-R8A
$REFLW          STRING  D4-BURMA/E2-VEST
$SECAN          STRING  D5-LEMON/F5-LEMON
$SILNITROP      STRING  CPNT685A
$STMOX          STRING  F8-ASPEN

001.000 STARTING_MATERIAL          Stage: START
        Location : DIFF
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```
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        Desc.    :
        Traceable:    Update Supply    Trace Supply  Update Dest.
Trace Dest.

             Part                                    Attribute
        001  WWEPIAA18                               PRIMARY
002.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZESCRBIP
        Title    : WAFER SCRIBE          --  105MM WAFERS
003.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZENIT5SG
        Title    :  ACTIVE EXPOSE AND ETCH
004.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEFLD5DM
        Title    : DMOS/ FIELD OX AND NTR REMOVAL
005.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZENRONDMS
        Title    : N+ IMPLANT/GATE OXIDATION MODULE DMOS
006.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEPDP3SG
        Title    : 3u SAG W/POLY DEP/PHOS & IMPL.
007.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEPLY5DMS
        Title    : POLY EXPOSE & ETCH DMOS
008.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEPBDYIM
        Title    : P BODY & P+AVALANCHE IMPLANT/DRIVE MODULE
009.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEPSD5SG
        Title    : P+S/D EXPOSE AND IMPLANT
010.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZENSD5SG
        Title    : N+S/D MASK AND IMPLANT 6u
011.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEIDODMO
        Title    : INTERLAYER DOPED OXIDE/WITHOUT ARGON IMPLANT
012.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZECTN5SG
        Title    : CONTACT STEPPER & ETCH  5u (NO CRSI)
013.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEBSCONTACT
        Title    : BACKSIDE CONTACT MODULE FOR HIGH POWER MOSFET
014.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEMLODMS
        Title    : METAL DEP $MTLDP1   LIFTOFF
015.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEPADBIP
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016.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEFANEAL
        Title    : FINAL ANNEAL MODULE                  450 DEG
017.000 CALL_PROCEDURE                Stage:                DEFAULT
        Procedure: ZEKETHLY
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018.000 CALL_PROCEDURE              Stage:              DEFAULT
        Procedure: ZEBGRALL
        Title     : BACKGRIND MODULE - all processes
019.000 CALL_PROCEDURE              Stage:              DEFAULT
        Procedure: ZEBSMETAL
        Title     : METAL DEP WAFER BACKSIDE (CALL ENG)
020.000 CALL_PROCEDURE              Stage:              DEFAULT
        Procedure: ZEFINVIS
        Title     : Final Visual Inspection w/o pop.
021.000 CALL_PROCEDURE              Stage:              DEFAULT
        Procedure: ZETRNFER
        Title     : WAFER TRANSFER
022.000 MOVE_TO_LOCATION            Stage: ENGINV
        Location : ENGINV
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**********************************************************************
**********
Procedure       : WTCBS-001A.04                          PLANNABLE
Title           : 5µ DMOS W/BSCONTACT HIGH POWER MOSFET 150MM
Owner           : FIX                          Date created     : [illegible]
[illegible] 08:00
Status          : ACTIVE NOSTARTS              Date last changed: [illegible]
[illegible]16:29
Access category:                               Date activated   : [illegible]
[illegible] 09:48
Procedure usage: PRIMARY_PROCEDURE             Main prod area   : WAFERFAB
ECN             :
Document        : DEVICE          WTCBS-001A.04

                        Material constraints
       Identity     Processing state Main-Material type Sub-Material
type
Entry: Nothing      Nothing          Nothing            Nothing
Exit : Identified   Normal           W = wafers         Nothing

No category has been specified.

No output part has been specified.

No material type conversions have been specified.


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$CAPOX          STRING  08-ORCID
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                Exit constraint:  NOCHANGE/NOCHANGE/NOCHANGE/NOCHANGE
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$FNLPAS         STRING  4KOX_4KNIT
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